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LT-5 reissue

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION FOR REISSUE
OF U.S. PATENT 4,823,070

Date of Issue	:	April 18, 1989
Inventor	:	Carl T. Nelson
Title	:	SWITCHING VOLTAGE REGULATOR CIRCUIT
Assignee	:	Linear Technology Corporation

Commissioner of Patents
and Trademarks
Washington, D.C. 20231

REISSUE DECLARATION AND POWER OF ATTORNEY

Sir:

I, CARL T. NELSON, the named inventor of United States patent 4,823,070, and the applicant for reissue thereof, declare that:

1. I am a citizen of the United States residing at 1167 Settle Avenue, San Jose, California 95125.

2. I have reviewed and understand the contents of the attached specification, including the claims, and verily believe that I am the original, first and sole inventor of the "Switching Voltage Regulator Circuit" invention described and claimed in that specification and for which a reissue patent is being sought.

3. I make this declaration under 37 C.F.R. 1.175 in support of this application for reissue.

4. Upon information and belief, United States patent 4,823,070 is partly inoperative by reason of my having claimed, as the patentee, less than I had a right to claim, in that those claims of the patent directed to an integrated circuit having "at most" five terminals include limitations that were not and are not required to distinguish patentably my invention over the prior art.

5. The particular errors in the patent which unnecessarily limit the claimed invention are the recitation, in each of the claims directed to an integrated circuit having "at most" five terminals for implementing a switching voltage regulator, of means for enabling or programming the integrated circuit to operate in an "isolated flyback mode" or for trimming a flyback voltage when the claimed integrated circuit operates in an "isolated flyback mode" (claims 1, 40 and 75-81), and/or means for selecting a mode of operation of the integrated circuit including an isolated flyback mode (claims 1 and 40), and/or means responsive to control signals applied to a multi-function terminal to perform a plurality of recited functions (claims 75-81). For example, these errors appear explicitly in independent claims 1, 40 and 75-81 as follows:

Claim	Limitation
1	"... second means ... for enabling the integrated circuit to operate in an isolated flyback mode ..."
	"... mode select means ... to disable the first means and enable the second means ..."
40	"... second means ... for enabling the integrated circuit to operate in a fully-

	isolated flyback mode ...."
	".. mode select means ... to disable one of the first and second means and to enable the other ..."
75-80	"... means for programming the integrated circuit to operate in one of a normal feedback mode and a fully-isolated flyback mode ..."
81	"... programming the integrated circuit to operate in one of a normal feedback mode and a fully-isolated flyback mode ..."
75, 78	"... second means ... for performing at least two of: ... frequency compensating ..., limiting peak current ..., variably limiting current .., and ... shutting down the integrated circuit ..."
76, 79	"... second means ... for: ... frequency compensating ..., limiting peak current ..., variably limiting current .., and ... shutting down the integrated circuit ..."
77, 80	"... second means ... for performing at least two of: ... frequency compensating ..., limiting peak current ..., and ... variably limiting current ..."
81	"... a second multi-function terminal .. for performing at least two functions selected from the group of: .. frequency compensating ..., ... limiting peak current ..., ... variably limiting current ..., and ... shutting down the integrated circuit ...".

The limitations of claim 40 are incorporated in claims 41-53 which depend directly or indirectly from that independent claim 40.

6. The foregoing errors arose, without any deceptive intention, through my efforts during preparation and prosecution of the applications for the '070 patent to particularly point out and distinctly claim my invention based upon my understanding of

the invention. The invention disclosed in the '070 patent was incorporated into a five-terminal current-mode switching voltage regulator integrated circuit product, designed by me and sold by the assignee of the '070 patent under the designation "LT-1070." The LT-1070 incorporates a power switching transistor, duty cycle control circuitry, error signal circuitry, comparator circuitry and a current sense resistor, thus making it simple to implement a switching regulator circuit with the LT-1070. I had also made the product versatile, despite its limited number of terminals, by assigning terminals multiple functions, and I also included circuitry to make the product operable in either normal feedback or isolated flyback mode. During preparation and prosecution of the applications for the '070 patent, I sought to and did claim my invention of a five terminal switching voltage regulator integrated circuit in terms of circuitry to enable operation in normal feedback and isolated flyback modes and/or in terms of multiple function terminals.

7. The true scope of the invention disclosed in the '070 patent, as claimed in new reissue claims 82-84, was not fully appreciated by me at the time the applications for the '070 patent were prepared and prosecuted. My invention of a current-mode switching voltage regulator integrated circuit having at most five terminals and incorporating a power switching transistor, duty cycle control circuitry, error signal circuitry, comparator circuitry and a current sense resistor, was not accomplished by any prior art switching voltage regulator integrated circuit product known to me. However, as set forth above, all of the

independent claims of the '070 patent directed to an integrated circuit having "at most" five terminals for implementing a switching voltage regulator recite, as unnecessary limitations, circuitry to enable operation in normal feedback and isolated flyback modes and/or multiple function terminals.

8. The foregoing errors were discovered during July-October, 1990, while the '070 patent was being studied by me, counsel for Linear Technology Corporation (the assignee of the '070 patent)) and Robert C. Dobkin (Vice President, Engineering, of Linear Technology Corporation), during a review of the patent in anticipation of litigation.

9. Newly presented claim 82 overcomes the defects of claims 1, 40 and 75-81 by claiming my invention in a way which eliminates the foregoing unnecessary limitations. In particular, new reissue claim 82 (the only independent claim being added by reissue) is directed to an integrated circuit for implementing a current-mode switching voltage regulator, the integrated circuit including (1) "at most" five terminals, as specifically recited for connection to external components; (2) a power switching transistor having its collector-emitter circuit coupled to conduct a current between the output terminal and the ground terminal; (3) means coupled to the switching transistor for varying the on and off duty cycle of the switching transistor in response to a control signal; (4) means including a resistive element coupled in series with the collector-emitter circuit of the switching transistor for generating a current sense signal indicative of the current conducted by the switching transistor; (5) means for

generating an error signal indicative of a difference between the feedback signal and a reference signal; (6) means for coupling the error signal to a function terminal; and (7) means for comparing the current sense signal to the error signal and for generating the control signal to turn off the switching transistor when the current sense signal compares in a predetermined manner to the error signal to vary the duty cycle of the switching transistor to produce the regulated output voltage.

10. New reissue claim 83, dependent from claim 82, adds that the control signal of new claim 82 is generated when the current sense signal equals or exceeds the error signal. New reissue claim 84, also dependent from claim 82, adds that the integrated circuit further includes means responsive to control signals applied to the frequency compensation terminal for performing at least one of: (a) limiting peak current conducted by the switching transistor, (b) variably limiting current conducted by the switching transistor as a function of time, and (c) shutting down the integrated circuit, whereby current drawn by the integrated circuit is reduced.

11. My invention, as claimed by new reissue claims 82-84, is fully disclosed in and supported by the specification of the '070 patent. For example, the '070 patent describes under the "Background Of The Invention" that "integrated circuits heretofore available typically required 8-14 terminals for connection to external discrete components .... This quantity of terminals prevents such integrated circuits from being packaged in low-cost power transistor packages such as the conventional 5-pin TO-3 type

metal can or the TO-220 type molded plastic packages ..." (column 2, lines 32-41). The patent specification goes on to state, under the heading "Summary Of The Invention", that the invention provides "a novel switching regulator circuit which can be packaged as an integrated circuit requiring only five external terminals for connection to discrete external components" (column 3, lines 14-18). The patent then shows and describes an exemplary embodiment of my invention as a "five-terminal integrated circuit ... capable of implementing a current-mode switching voltage regulator circuit, and capable of being packaged in a conventional 5-pin power package. Five terminals are shown, labeled as V_{IN} (input supply), V_{SW} (output), FB (feedback), V_C (compensation) and GND (ground)" (column 4, lines 4-10 et seq.; Figure 1). The patent goes on to describe how terminals FB and V_C may perform more than one function.

12. Two other specific errors in the '070 patent are printing errors by which the term -- peak -- was omitted from claim 73, column 31, at line 47 after "limiting", and the incorrect term "where" in claim 79, column 34, line 61, was substituted for the proper term -- whereby --. These errors, made by the Patent and Trademark Office when printing the '070 patent, arose without deceptive intent on my part and, upon information and belief, were discovered when the '070 patent was proofread. I believe that these errors render the '070 patent partly inoperative by reason of a defective specification.

13. I hereby acknowledge my duty to disclose to the Patent and Trademark Office information of which I am aware that

is material to the examination of this reissue application in accordance with Rule 56 of the Patent Office Rules (37 C.F.R. §1.56(a)).

14. I hereby appoint CHARLES B. SMITH, Reg. No. 16,763, and MARK D. ROWLAND, Reg. No. 32,077, both of Fish & Neave, 875 Third Avenue, New York, New York 10022-6250, telephone (212) 715-0600, as their principal attorneys of record in connection with the captioned patent, with full power to prosecute this application for reissue and to transact all business in the Patent and Trademark Office in connection therewith. All correspondence should be sent to Mark D. Rowland at the above address.

15. I hereby declare that I understand the English language, and that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements are made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of this application or any patent issued thereon.

Executed April 5, 1991

Carl T. Nelson

Carl T. Nelson